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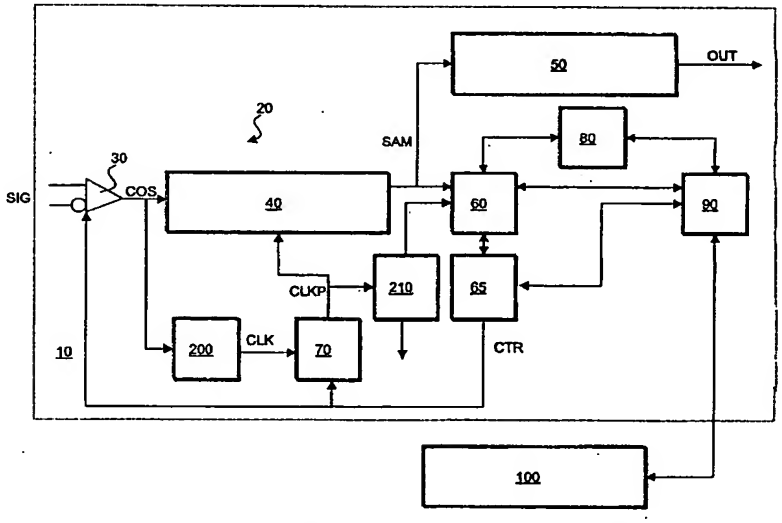
(54) Title: INTEGRATED CIRCUIT WITH BIT ERROR TEST CAPABILITY



(57) Abstract: An integrated circuit (10), preferably a field programmable gate array - FPGAor an application specific integrated circuit - ASIC -, comprises a level comparator (30) for comparing a level of a comparator input signal and correspondingly providing a comparator output signal (COS). A sampling unit (40) is coupled to the level comparator (30) for sampling (SAM) the comparator output signal (COS). A bit error test unit (60) receives the sampled comparator output signal (SAM) and determine therefrom an indication of a bit error in a sequence of the sampled comparator output signal (SAM).

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